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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/519,695	KIM ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-6 and 13-21 have been considered. Claims 7-12 have been cancelled as requested by the Applicant.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 13-16, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek).

5. Referring to claim 13, Pechanek has taught a computer system comprising:

   a. A processor having a very large word instruction architecture and including a plurality of clusters of functional processing units, each one cluster of the plurality of clusters comprising a common number of functional processing units, the processor comprising a first prescribed number of clusters (Pechanek column

4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3, elements 101, 151, 196, and 155)

b. Said very large word instruction architecture allowing an instruction to have up to a second prescribed number of subinstructions (Pechanek column 1, lines 39-42 and Figure 2), where the second prescribed number equals the first prescribed number times the common number, each instruction to be executed by the processor comprising from one subinstruction up to the second prescribed number of subinstructions, along with a set of control bits (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the first prescribed number equals the second prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. An instructions cache memory (Pechanek column 4, lines 54-56) which stores a first instruction in a compressed format determined by a condition of the set of control bits (Pechanek column 5, lines 61-65), the compressed format including a shared subinstruction stored in a given field of the first instruction which is to be shared by a plurality of the functional processing units (Pechanek column 9, lines 23-25 and Figure 4C), said plurality of functional processing units being determined by said condition of the set of control bits (Pechanek column 9, lines 28-30 and Figure 4C).

6. Referring to claim 14, Pechanek has taught said shared subinstruction is for a first functional processing unit of a first cluster and a first functional processing unit of a second cluster when the set of control bits identifies a first prescribed condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33). In regards to Pechanek, part of the control bits determine whether the instructions being sent are active and need to be loaded and executed by the units.

7. Referring to claim 15, Pechanek has taught shared subinstruction is a first shared subinstruction, and in which the compressed format further includes a second shared subinstruction for a second functional processing unit of the first cluster and a second functional processing unit of the second cluster when the set of control bits either concurrently identifies a second prescribed condition (Pechanek column 10, 44-54).

8. Referring to claim 16, Pechanek has taught:

a. Means for testing the set of control bits for a given instruction (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the device must test certain control bits in order to determine whether to execute certain types of instructions, and it must also pre-decode the instruction, which identifies the prescribed condition.

b. Means for routing said first common subinstruction to the first functional processing unit of the first cluster and to the first functional processing unit of the second cluster of the plurality of clusters when said testing means identifies the first prescribed condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33).

9. Referring to claim 19, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster (Pechanek column 2, lines 24-27), the system further comprising means for compressing the first instruction into the compressed format

b. Means for testing the set of control bits associated with the first instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

c. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

10. Referring to claim 20, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster

(Pechanek column 2, lines 24-27), the system further comprising means for compressing the first instruction into the compressed format

b. Means for testing the set of control bits associated with the first instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

c. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

d. Means for loading the first instruction into the instruction cache in the compressed format (Pechanek column 4, lines 54-56).

Claim Rejections - 35 USC § 103

11. Claims 1-3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition by Jerry M. Rosenberg © 1987 (herein referred to as Rosenberg).

12. Referring to claim 1, Pechanek has taught a method for sharing a subinstruction of a given instruction among functional processing units of a plurality of clusters on a processor having a very long instruction word architecture (Pechanek column 4, lines 42-49; columns 4-5, clines 67-1; column 5, lines 31-32; and Figure 3, elements 101, 151, 153, and 155), the given instruction including a set of control bits (Pechanek column 6, lines 43-44; column 9, lines 24-33; and Figure 4C, elements 455) and at least one subinstruction (Pechanek column 1, lines 39-

41 and Figure 2), the processor comprising the plurality of clusters, each one cluster of the plurality of the comprising a plurality of functional processing units (Pechanek columns 4-5, lines 67-1; column 2, lines 24-27; and Figure 3). The method comprising the steps of:

a. Testing the set of control bits to identify a prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the device must test certain control bits in order to determine whether to execute certain types of instructions, and it must also pre-decode the instruction, which identifies the prescribed condition.

b. When the prescribed condition is identified, routing said subinstruction of the given instruction to multiple functional processing units as determined by the prescribed condition (Pechanek column 10, lines 44-54). In regards to Pechanek, part of the control bits determine whether the instructions being sent are active and need to be loaded and executed by the units.

13. Pechanek has not explicitly taught concurrently executing the subinstruction at said multiple functional processing units. However, Pechanek has taught parallel processing in his device (Pechanek column 1, lines 1-18 and 36-37). Rosenberg has taught parallel processing is the concurrent execution of multiple processes in a single unit (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

14. Referring to claim 2, Pechanek has taught routing said subinstruction of the given instruction to a first functional processing unit of a first cluster of the plurality of clusters and to a first functional processing unit of a second cluster of the plurality of clusters (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33).

15. Pechanek has not explicitly taught concurrently executing the subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and to the first functional processing unit of the second cluster of the plurality of clusters. Rosenberg has taught concurrently executing the subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and at the first functional processing unit of the second cluster of the plurality of clusters (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

16. Referring to claim 3, Pechanek has taught a method:

a. In which the given instruction comprises a first subinstruction and a second subinstruction (Pechanek column 1, lines 39-41 and Figure 2).

b. The step of testing comprising testing the set of control bits to identify a first prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the bits must be tested in order to identify the instruction.

c. The step of routing comprising routing the first subinstruction (Pechanek column 10, lines 44-54). In regards to Pechanek, the first subinstruction must be routed in order to be inputted to the decoder and execution unit.

d. Testing the set of control bits to identify a second prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the bits must be tested in order to identify the instruction.

e. When the second prescribed condition is identified, routing said second subinstruction of the given instruction to a second functional processing unit of the first cluster of the plurality of clusters and to a second functional processing unit of the second cluster of the plurality of clusters (Pechanek column 10, 44-54). In regards to Pechanek, the subinstruction must be routed in order for it to be inputted to another decode and execution unit.

17. Pechanek has not explicitly taught:

a. Concurrently executing the subinstruction at the first functional processing unit and the second functional processing unit

b. Wherein the step of executing comprises concurrently executing the first subinstruction at the first functional processing unit of the cluster, the first subinstruction at the first functional processing unit of the second cluster, the second subinstruction at the second functional processing unit of the first cluster

and the second subinstruction at the second functional processing unit of the second cluster.

18. However, Pechanek has taught a device capable of parallel processing (Pechanek column 1, lines 17-18 and 36-37 and column 11, lines 28-33). Rosenberg has taught:

a. Concurrently executing the subinstruction at the first functional processing unit and the second functional processing unit (Rosenberg page 452, element "parallel processing").

b. Wherein the step of executing comprises concurrently executing the first subinstruction at the first functional processing unit of the cluster, the first subinstruction at the first functional processing unit of the second cluster, the second subinstruction at the second functional processing unit of the first cluster and the second subinstruction at the second functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing").

19. In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

20. Referring to claim 17, Pechanek has not explicitly taught the first common subinstruction is concurrently executed at the first functional processing unit of the first cluster and the first functional processing unit of the second cluster. However, Pechanek has taught a device capable

of parallel processing (Pechanek column 1, lines 17-18 and 36-37 and column 11, lines 28-33). Rosenberg has taught the first common subinstruction is concurrently executed at the first functional processing unit of the first cluster and the first functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

21. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Tsushima et al., U.S. Patent Number 6,044,450 (herein referred to as Tsushima) and in further view of Miller et al., U.S. Patent Number 5,819,058 (herein referred to as Miller).

22. Referring to claims 4 and 5, Pechanek has taught a method:

a. Wherein each instruction comprises at least one subinstruction and up to a first prescribed number of instructions, the first prescribed number being at least two (Applicant's claim 4) (Pechanek column 1, lines 39-42 and Figure 2)

b. Wherein the processor is organized into a plurality of clusters equaling a second prescribed number, each one cluster of the plurality of clusters comprising a common number of functional processing units, wherein the common number of functional processing units times the second prescribed number equals the first

prescribed number (Applicant's claim 4) (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the second prescribed number equals the first prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. Wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction (Applicant's claim 4) (Pechanek column 9, lines 52-58; Figure 3; and Figure 8).

d. When the pattern is among the set of prescribed patters, setting a set of control bits for the instruction to indicate that said pattern is present (Applicant's claim 4) (Pechanek column 5, lines 61-65; column 6, lines 32-44; column 9, lines 24-33; and Figure 4C, element 455).

e. Pechanek has taught compressing the given instruction when the pattern is among the set of prescribed patterns by deleting one occurrence of the redundant subinstruction in the given instruction to achieve a compressed instruction (Applicant's claim 5) (Pechanek column 3, lines 54-56).

23. Pechanek has not explicitly taught

a. Identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction

b. Determining whether the pattern is among a set of prescribed patterns

24. However, Pechanek has taught compressing the instruction (Pechanek columns 8-9, lines 66-1). Tsushima has explicitly taught a compression method:

a. Identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction (Applicant's claim 4) (Tsushima column 7, lines 58-64). In regards to Tsushima, in order to divide the instruction into groups, a pattern must be indentified in the instruction and more than once.

b. Determining whether the pattern is among a set of prescribed patterns (Applicant's claim 4) (Tsushima column 7, lines 61-65). In regards to Tsushima, in order to set the group codes, the pattern must be matched with the existing group codes.

25. It would have been obvious to a person of ordinary skill in the art to incorporate the above method of Tsushima, because it is part of a compression method. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the compression method of Tsushima in the device of Pechanek.

26. In addition, Pechanek has not explicitly taught the compression method executing during compilation of the computer program (Applicant's claims 4 and 5). However, Pechanek has taught compressing the instruction (Pechanek columns 8-9, lines 66-1). Miller has taught executing a compression method executing during compilation of the computer program (Applicant's claims 4 and 5) (Miller column 6, lines 57-58). It would have been obvious to a person of ordinary skill in the art to incorporate the compression method during compilation of

the computer program, because, during compilation of the computer program, the instructions are translated so the processor will be able to execute the commands and the commands are stored. When the instructions are compressed during compilation, not as much memory is wasted while the translated commands are being stored, and the compression process does not have to be performed during actual program execution, thereby increasing processor time and decreasing processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compression method during compilation of the computer program in the device of Pechanek.

27. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek in view of Tsushima and in further view of Miller as applied to claims 4-5 above, and further in view of Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition by Jerry M. Rosenberg © 1987 (herein referred to as Rosenberg). Pechanek has taught:

a. Moving the compressed instruction into an instruction cache (Pechanek column 4, lines 54-56).

b. Testing the set of control bits of the compressed instruction to determine a condition is identified in which subinstruction sharing is to occur for the compressed instruction (Pechanek column 10, lines 44-54).

c. When subinstruction sharing is determined to occur, parsing the compressed instruction to route the redundant subinstruction to a plurality of functional processing units as determined by the identified condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; column 11, lines 28-33; and Figure 3).

28. Pechanek has not explicitly taught concurrently executing the subinstruction at said plurality of functional processing units. (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

29. Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Colwell et al., U.S. Patent Number 5,057,837 (herein referred to as Colwell).

30. Referring to claim 18, Pechanek has taught:

a. The first instruction in an uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster, the system further comprising means for compiling the first instruction (Pechanek column 1, lines 39-42; column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; column 9, lines 52-58; Figure 2; Figure 3; and Figure 8).

b. Means for setting a state of the set of control bits to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Pechanek column 5, lines 61-65).

31. Pechanek has not explicitly taught means for comparing the first subinstruction and the second subinstruction. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising means for comparing the first subinstruction and the second subinstruction (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, which includes means for comparing the first and second subinstructions, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

32. Referring to claim 21, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster (Pechanek column 2, lines 24-27), the system further comprising means for caching the first instruction (Pechanek column 4, lines 54-56).

b. Mean for setting a state of the set of control bits associated with the first instruction to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Pechanek column 5, lines 61-65).

c. Means for reducing the size of the first instruction to achieve a compressed format by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

d. Means for loading the first instruction into the instruction cache in the compressed format Pechanek column 4, lines 54-56).

33. Pechanek has not explicitly taught means for comparing the first subinstruction and the second subinstruction. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising means for comparing the first subinstruction and the second subinstruction (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, which includes means for comparing the first and second subinstructions, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

Response to Arguments

34. The examiner withdraws the objection to the declaration in favor of the substitute declaration.

35. The examiner withdraws the objection to the specification in favor of the new specification page 16.

36. The examiner withdraws the objections to claims 2, 5, and 6 in favor of the amended claims.

37. The examiner has considered the Applicant's arguments in Amendment A filed on 5 March 2003, but they have not been found persuasive.

38. Applicants argue on page 1 essentially that:

> "There is no disclosure or suggestion of allocating subinstructions of a common VLIW into execution units across multiple PE's. Accordingly, there is no disclosure or suggestion of loading a subinstruction of a given VLIW into functional units of multiple clusters."

39. This has not been found persuasive. Pechanek shows in Figure 3 an instruction bus from the I-Fetch Unit 103 connecting to all PE's and feeding them common subinstructions of a common VLIW instruction (Pechanek columns 2-3, lines 61-4 and column 4, lines 49-58). Each of the units loads and stores the subinstruction for execution in the individual units.

40. Applicants argue on page 5 essentially "Pechanek does not disclose or suggest compressing subinstructions." This has not been found persuasive. Pechanek has taught removing duplicate subinstructions (Pechanek Abstract, lines 12-16 and 20-26; column 2, lines 12-27; and column 3, lines 54-59), thereby compressing the subinstructions and using less memory space.

41. Applicants argue on pages 5, 6, 6-7, and 8 essentially that:

> "Of significance here, is that there are no control bits in the loaded VLIW instruction which determine how the subinstructions of such loaded VLIW instruction are to be allocated among execution units."

42. This has not been found persuasive. Pechanek has taught different execution units accessing different parts, internal memory, and decode unit, which determines where instructions are sent (Pechanek Figure 3, elements Instruction Decode and SLAMD and columns 4-5, lines 59-9). It is known in the art that instructions include control codes, also called operation codes or op-codes, composed of bits that ID the type of instruction it is, so that the proper unit and method will execute the instruction. The decoder separates the instructions and sends them to the proper instruction unit, and this is normally done based on the control codes. Also, the separate instruction referred to in the applicants' arguments do not determine the routing of the subinstructions, just which address is to be executed not where instructions reside or which unit executes it (Pechanek Figure 4 and columns 5-6, lines 57-4).

43. Applicants argue on pages 6 and 8 essentially that:

> "Claim 14 further distinguishes over the cited art...
>
> - in which said shared subinstruction is for a first functional processing unit of a first cluster and a first functional processing unit of a second cluster when the set of control bits identifies a first prescribed condition.
>
> ...In Pechanek a given subinstruction of a loaded VLIW instruction is only routed to execution units within the same PE."

44. This argument has not been found persuasive. Pechanek shows in Figure 3 that the instruction bus from I-Fetch 103 connects to all PE's and feeding them common subinstructions (Pechanek columns 2-3, lines 61-4.and column 4, lines 49-58). The same subinstruction are fed to the PE's and then the corresponding functional units in the PE's process the instruction, because, since each functional unit processes a certain type of instruction, they will correspond to the same subinstructions.

45. Applicants argue on page 6 essentially that "Claim 15 further distinguishes over the cited art by reciting that second subinstruction is shared among functional processing units of a first cluster and a second cluster." This argument has not been found persuasive. Pechanek has taught that VLIW instructions contain at least 1 instruction (Pechanek Figure 2 and columns 1-2, lines 36-11) and Pechanek's Figure 3's I-Fetch Unit 103 fetches subinstructions that are sent to the PE's (Pechanek columns 2-3, lines 61-4 and column 4, lines 49-58).

46. Applicants argue on page 6 essentially that "Claim 16 further distinguishes over the cited art by including means for routing the subinstruction to...the first cluster and...the second cluster." This argument has not been found persuasive. Pechanek shows in Figure 3 an instruction bus for routing the subinstruction fetched by the I-Fetch Unit 103 to separate clusters.

47. Applicants argue on page 7 essentially that:

> "Parallel processing means there is concurrent processing. It does not by definition mean that pipelines are synchronized to assure that the same subinstruction routed to two separate clusters is processed at the same time – rather than 1 or more clock cycles before or earlier."

48. This argument has not been found persuasive. The pipelines in Pechanek are synchronized to execute the same subinstruction at the same time. The synchronization is controlled by the execute-VLIW subinstructions, which specify which subinstructions are executed and when the subinstructions are executed, but not where the subinstructions are routed and stored (Pechanek Figure 4B and columns 5-6, lines 57-4).

49. Applicant's arguments with respect to claims 4-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

51. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

53. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

54. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

April 28, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100